REMARKS

The above-identified patent application has been reviewed in light of the Examiner's Final Office Action dated April 9, 2007. Claims 1 and 4 have been amended, without intending to abandon or to dedicate to the public any patentable subject matter. Accordingly, Claims 1-21 are now pending. As set forth herein, reconsideration and withdrawal of the rejections of the claims are respectfully requested.

Initially, applicant notes that the amendments to Claims 1 and 4 correct typographical errors. Accordingly, it is submitted that Claims 1 and 4 should be entered.

Claims 1-5, 7, 10-13, and 16-19 stand rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,619,698 to Lillich et al. ("Lillich"). In addition, Claims 6, 8, 9, 14, 15, 20, and 21 stand rejected under 35 U.S.C. § 103 as being obvious over Lillich in view of U.S. Patent Application Publication No. 2004/0107416 to Buban et al. ("Buban"), Lillich in view of U.S. Patent Application Publication No. 2003/0167463 to Munsil et al. ("Munsil"), or U.S. Patent Application Publication No. 2002/0152455 to Hundt et al ("Hundt") in view of Buban. In order for a rejection under 35 U.S.C. § 102 to be proper, each and every element as set forth in the claim must be found, either expressly or inherently described, in a single prior art reference (MPEP § 2131). In order to establish a *prima facie* case of obviousness under §103, there must be some suggestion or motivation to modify the reference or to combine the reference teachings, there must be a reasonable expectation of success, and the prior art reference or references must teach or suggest all of the claim limitations (MPEP § 2143). However, all of the claim elements cannot be found in the cited references, whether those references are considered alone or in

combination. Accordingly, reconsideration and withdrawal of the rejections of the claims as anticipated by or obvious in view of the cited references are respectfully requested.

The primary reference, Lillich, contains a discussion of a conventional patch arrangement, in which an ATRAP instruction is used to cause a processor to halt execution of a set of instructions, and to store state information for those instructions. The microprocessor then resumes execution at a low memory location, which is the address of the TRAP dispatcher. The TRAP dispatcher then examines the ATRAP instruction to determine what the operation stands for, looks up the operation of the corresponding system routine in the TRAP table, and then jumps to that corresponding system routine. (Lillich, column 2, line 24 to column 3, line 5.). In contrast, pending Claim 1 recites "injecting a jump instruction and an address of an update table at a location in a memory containing a first instruction of a first replaced function." Accordingly, the method recited by Claim 1 recites a number of aspects that are not disclosed by Lillich.

In particular, Lillich does not disclose injecting a jump instruction and an address of an update table at a location in memory containing a first instruction of a first replaced function. The ATRAP instruction in Lillich that the Office Action equates to the injected jump instruction simply causes the processor to halt execution of application code, store state information, and resume execution at an address indicated in a low memory location (and not by the ATRAP instruction) which is the address of the TRAP dispatcher. (Lillich, column 2, lines 48-54.) Accordingly, Lillich does not teach, suggest or describe injecting a jump instruction and an address of an update table as claimed.

In addition, Lillich does not disclose injecting a jump instruction at a location in a

memory containing a first instruction of a first replaced function. In particular, the ATRAP instruction cited by the Office Action in connection with this aspect of Claim 1 is not in a location of a first instruction of a first replaced function. Instead, the ATRAP instruction is encountered during execution of application code. (Lillich, column 2, lines 48-49.) This is illustrated in Fig. 2 of Lillich, where the ATRAP instruction is shown included in the body of application code 102. Moreover, the system routine 122 that is illustrated by Lillich as being replaced is not altered as part of a patch operation. Instead, address 1 in the TRAP table 110 is altered to point to the patch code instead of the replaced code. (Lillich, column 3, lines 15-50; Fig. 2.) Therefore, Lillich does not disclose injecting a jump instruction at a location in memory containing a first instruction of a first replaced function as recited by Claim 1. Moreover, as indicated by lines 152 and 148, after executing the patch code, execution resumes immediately following the ATRAP instruction in the application code 102. (Lillich, Fig. 2.) This is further confirmation that the ATRAP instruction is not injected at the location of a first instruction of a first replaced function as claimed.

Claim 10 recites a computer implemented method that includes injecting in said running executable program to be patched at a location in said memory containing a first instruction of said function to be replaced a jump instruction and an address of a new function. As explained elsewhere herein, Lillich does not contain a description of injecting a jump instruction and an address for new function at a location in memory containing a first instruction of a function to be replaced. Accordingly, the rejections of Claim 10 and dependent Claims 11-17 should be reconsidered and withdrawn.

Claim 18 is generally directed to a system for updating executable program code. The system includes means for inserting a jump code and an address associated with a replacement function in place of an address of said function to be replaced in said existing executable program code. Lillich does not disclose changing an address in the executable code. Instead, Lillich discusses changing addresses in a TRAP table. Accordingly, the rejections of Claims 18 and 19 should be reconsidered and withdrawn.

The Buban and Munsil references that are cited in connection with rejections of various dependent claims do not teach, suggest or describe those elements of independent Claims 1 and/or 18 that are absent from Lillich. In addition, Buban does not discuss a predetermined distance between memory addresses and populating an update table with the address of the first updated function in response to determining that the first distance is at least the predetermined amount. Instead, Buban discusses preferably limiting the size of the instruction being updated to the processor's smallest unit of automatically replaceable memory. (Buban, paragraph 46.) Therefore, neither Lillich nor the Buban reference teaches, suggests or discloses the elements of Claims 6, 8, 14 and 15, and the rejections of these claims should be reconsidered and withdrawn.

The Munsil reference is cited in connection with a second memory space that is read-only memory space. However, Munsil does not teach, suggest or describe injecting a jump instruction and an address of an update table at a location in a memory containing a first instruction of a first replaced function as claimed. Accordingly, the rejection of Claim 9 should be reconsidered and withdrawn for at least these reasons.

The Office Action rejects Claims 20 and 21 as being obvious over Hundt in view of

Buban. Claim 20 recites a system for updating executing program code that includes a signal handler tool operable to replace in memory an address of the function to be replaced with the address of the replacement function. The replacement is performed in response to the instruction pointer being at least a predetermined distance from the address for the replacement function. Claim 21 depends from Claim 20.

The Hundt reference discusses using original functions to generate instrumented functions in executing the instrumented functions in place of the original functions. (Hundt, paragraph 18.) The Office Action acknowledges that there is no disclosure in Hundt related to making such a replacement in response to the position of the instruction pointer being at least a predetermined distance from the address of the replacement function. For such a disclosure, the Office Action cites Buban. However, as previously noted, Buban in fact contains no teaching, suggestion or disclosure of such a pre-determined distance. Therefore the rejections of Claims 20 and 21 should be reconsidered and withdrawn.

The application now appearing to be in condition for allowance, early notification of same is respectfully requested. The Examiner is invited to contact the undersigned by telephone if doing so would be of assistance.

Respectfully submitted,

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